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Warren Stuart Crippen

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/074,003	Applicant(s) CRIPPEN, WARREN STUART	
	Examiner Ishwar (I. B.) Patel	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-15, 18 and 19 is/are pending in the application.
- 4a) Of the above claim(s) 18 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 18 and 19 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The newly added claims are directed to a test card assembly comprising a test card printed circuit board, a probe head and a space transformer to be used in testing electrical characteristic. The original claims, claims 10-15 are drawn to a structure of a space transformer, which can be used in test assembly or in a semiconductor package for connecting semiconductor dies / devices or even as a printed circuit board. The newly added claims are classified in class 324/254+ and need a separate search than that of the original claims, which are directed to a structure. As such, the newly added claims and the original claims are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not need the details such as the adhesion promotion layer or the detail of the via connections. The subcombination has separate utility such as an interposer in a semiconductor package or as a circuit board for mounting a component.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for

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prosecution on the merits. Accordingly, claims 18 and 19 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoda et al., US Patent No. 6,661,088, (Yoda).

Regarding claim 10, Yoda, in an embodiment of figure 2, discloses a space transformer comprising: a silicon medium (silicon substrate 20) having a land grid array side (side of 20 facing package substrate 5) and a semiconductor side (side of 20 facing chip 1) opposite the land grid array side; and a predetermined contact pattern (pattern of contacts with vias 27) comprising electrically conductive material (copper, shown as first wiring layer 21 in figure 6A-6B, in more detail, column 6, line 58-67) disposed in an inner region of the silicon medium and defining electrical contact zones (contact zone of via 27, shown in more detail in figure 7B) providing double-sided electrical contacts (see 51,21, figure 7B) for the space transformer, the contact comprising: land grid array side

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contacts (11) disposed on the land grid array side of the silicon medium and having their largest dimension and their pitch in the order of mils to define a macro-pitch scale (electrodes 11 arranged with a pitch of 25 mil (250 μm), column 7, line 50-55, defining macro-pitch scale); and semiconductor side contacts (opening 51 of via 27) disposed on the semiconductor side of the silicon medium and having their largest dimension and their pitch in the order of microns to define a micro-pitch scale (pitch of via 27 is about 10 μm to 20 μm , column 5, line 5-10, defining micro-pitch scale), the electrical contact zones being disposed to convert a macro-pitch scale of the land grid array side contacts to the micro-pitch scale of the semiconductor side contacts (see 11 and 27 of element 3 in figure 2).

Regarding the recitation, “the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”, the language “being configured to be connected to corresponding ones of contacts” only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, Yoda anticipates the claim.

4. Claims 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoda et al., US Patent No. 6,661,088, (Yoda).

Regarding claim 10, Yoda, in an embodiment of figure 11A-11B, discloses a space transformer comprising: a silicon medium (silicon substrate 20) having a land grid array side (side of 20 facing package substrate 5, as shown in detail in figure 2) and a semiconductor side (side of 20 facing chip 1, as shown in detail in figure 2) opposite the land grid array side; and a predetermined contact pattern (pattern of contacts with vias 27) comprising electrically conductive material (copper, shown as first wiring layer 21 in figure 6A-6B, in more detail, column 6, line 58-67) disposed in an inner region of the silicon medium and defining electrical contact zones (contact zones of via 27 of first interposer layer 3-1) providing double-sided electrical contacts for the space transformer, the contact comprising: land grid array side contacts (11) disposed on the land grid array side of the silicon medium and having their largest dimension and their pitch in the order of mils to define a macro-pitch scale (electrodes 11 arranged with a pitch of 25 mil (250 μm), column 7, line 50-55, defining macro-pitch scale); and semiconductor side contacts disposed on the semiconductor side of the silicon medium and having their largest dimension and their pitch in the order of microns to define a micro-pitch scale (pitch of via 27 is about 10 μm to 20 μm , column 5, line 5-10, defining micro-pitch scale), the electrical contact zones being disposed to convert a macro-pitch scale of the land grid array side contacts to the micro-pitch scale of the semiconductor side contacts (see 11 and 27 of element 3 in figure 2).

Regarding the recitation, "the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly" and "the semiconductor side contacts further

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being configured to be connected to corresponding ones of a probe head of the test card assembly”, the language “being configured to be connected to corresponding ones of contacts” only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, Yoda anticipates the claim.

Regarding claim 11, Yoda, further discloses the silicon medium comprises a first silicon layer (silicon layer 20 in first interposer 3-1) and a second silicon layer (silicon layer 20 in first interposer 3-2), the contact pattern (pattern of via 27) being disposed between the first silicon layer and the second silicon layer.

Regarding claim 12, Yoda, further discloses the second silicon layer defines at least one via (via 27 in second interposer 3-2) therein, at least some of the electrically conductive material (copper, shown as first wiring layer 21 in figure 6A-6B, in more detail, column 6, line 58-67) being located in the at least one via.

Regarding claim 13, Yoda, further discloses an adhesion promoter (41, as shown in more detail in figure 5A) disposed between the electrically conductive material (copper, shown as first wiring layer 21 in figure 6A-6B, in more detail, column 6, line 58-67) and the first silicon layer (silicon layer 20 of first interposer).

5. Claims 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoda et al., US Patent No. 6,661,088 (Yoda).

Regarding claim 14, Yoda, in an embodiment of figure 11A-11B, discloses a space transformer comprising: a silicon medium (silicon substrate 20) having a land grid array side (side of 20 facing package substrate 5, as shown in detail in figure 2) and a semiconductor side (side of 20 facing chip 1, as shown in detail in figure 2) opposite the land grid array side; and further comprising: a first silicon layer (silicon layer 20 in first interposer 3-1) defining a plurality of vias (27) therein and a second silicon layer (silicon layer 20 in first interposer 3-2), disposed on the first silicon layer; a predetermined contact pattern (contact pattern of via 27 formed of copper film 49, shown in more detail in figure 6A-6B) comprising copper (copper film 49, column 6, line 57-58) and being disposed in an inner region located between the first silicon layer and the second silicon layer, at least some of the copper being disposed in the plurality of vias (27) for defining electrical contact zones (contact zone of via 27 exposed on the upper surface of first interposer layer 3-1) providing double-sided electrical contacts for the space transformer; the contacts comprising: land grid array side contacts disposed on the land grid array side of the silicon medium and having their largest dimension and their pitch in the order of mils to define a macro-pitch scale (electrodes 11 arranged with a pitch of 25 mil (250 μm), column 7, line 50-55, defining a macro-pitch scale); and semiconductor side contacts disposed on the semiconductor side of the silicon medium and having their largest dimension and their pitch in the order of microns to define a micro-pitch scale (pitch of via 27 is about 10 μm to 20 μm , column 5, line 5-10, defining

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a micro-pitch scale), the electrical contact zones (contact zone of via 27 of first interposer 3-1) being disposed to convert a macro-pitch scale of the land grid array side contacts to the micro-pitch scale of the semiconductor side contacts (see 11 and 27 of element 3 in figure 2).

Regarding the recitation, "the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly" and "the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly", the language "being configured to be connected to corresponding ones of contacts" only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, Yoda anticipates the claim.

Regarding claim 15, Yoda, further discloses a layer of adhesion promoter (41, as shown in more detail in figure 5A) disposed between the electrically conductive material (copper) and the first silicon layer (20 of first interposer 3-1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 10-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Pham et al., US Patent No. 6,303,992, (Van) in view of Eldridge et al., US Patent No. 5,974,662 (Eldridge).

Regarding claim 10, Van, in of figure 4, discloses a space transformer comprising: a silicon medium (12, made of silicon, column 3, line 41-49) having a land grid array side (side facing substrate 70) and a semiconductor side (side facing semiconductor die 50) opposite the land grid array side; and a predetermined contact pattern (pad 18, 20 and vertical and horizontal conductive conduits 22, column 3, line 1-8) comprising electrically conductive material (copper, column 4, line 1-10) disposed in an inner region of the silicon medium and defining electrical contact zones (contact zones of conduit 22 with pads 18, 20) providing double-sided electrical contacts for the space transformer, the contact comprising: land grid array side contacts (20) disposed on the land grid array side of the silicon medium and semiconductor side contacts (18) disposed on the semiconductor side of the silicon medium.

Van fails to explicitly disclose land grid array side contacts have their largest dimension and their pitch in the order of mils to define a macro-pitch scale and semiconductor side contacts having their largest dimension and their pitch in the order of microns to define a micro-pitch scale. However, Van discloses a space transformer made of ceramic material such as silicon with land grid array side contacts (20) directly connected to the pads 72 of the substrate, (see description on column 3, line 56-64) and semiconductor side contacts (18) directly connected to the pads 54 of the die 50,

(column 3, line 41-49). This implies that the space transformer of Van Pham et al., is converting the dimension of land grid array side contacts (20), which match to that of the substrate to the dimension of semiconductor side contacts (18), which match to that of the semiconductor.

Further, Eldridge, in figure 4, discloses a space transformer 400, made of ceramic, with bottom surface 402b with terminals at a 50-100 mil pitch, comparable to printed circuit board pitch, (land grid array side), defining macro-pitch scale, and top surface 402a with a relatively fine pitch, about 127 micron to 254 micron (5-10 mil pitch), center to center spacing comparable to semiconductor die bond pad, defining a micro-pitch scale, see column 23, line 5-25.

A person of ordinary skill in the art at the time the invention was made would readily construe that the dimension, size and spacing, on printed wiring board side, land grid array side would be larger, with wider pitch, defining a macro-pitch scale, than that on the semiconductor side contacts of a space transformer, with narrower pitch, defining a micro-pitch scale, for connecting a semiconductor device on one side of the space transformer and a printed circuit board on the other side of the space transformer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to construe the space transformer of Van with land grid array side contacts having dimensions and spacing larger, defining a macro-pitch scale, than that on the semiconductor side contacts, defining a micro-pitch scale, from the

teachings of Eldridge, in order to facilitate connection of the semiconductor device on one side and the printed circuit board on the other side of the space transformer.

Regarding the recitation, “the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”, the language “being configured to be connected to corresponding ones of contacts” only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, the modified structure of Van anticipates the claims.

Regarding claim 11, Van further discloses the silicon medium comprises a first silicon layer and a second silicon layer, the contact pattern (conductive conduits 22, column 3, line 1-8) being disposed between the first silicon layer and second silicon layer, (see figure 4 and 8A-B, column 4, line 60 to column 5, line 5).

Regarding claim 12, Van further discloses the second conductive layer defines at least one via (via 22) therein, at least some of the electrically conductive material being located in the least one via (see figure 4, column 4, line 1-5).

Regarding claim 14, Van, in figure 4, discloses a space transformer comprising: a silicon medium (12, made of silicon, column 3, line 41-49) having a land grid array side (side facing substrate 70) and a semiconductor side (side facing semiconductor die 50) opposite the land grid array side; and further comprising: a first silicon layer (silicon layer below the horizontal conduit 22) defining a plurality of vias (holes in the silicon layer below the horizontal conduit 22) therein and a second silicon layer (silicon layer above the horizontal conduit 22), disposed on the first silicon layer; a predetermined contact pattern (via hole and conduit 22 and pads 18 and 20) comprising copper (copper, column 4, line 1-10) and being disposed in an inner region located between the first silicon layer and the second silicon layer, at least some of the copper being disposed in the plurality of vias (vertical conduit 22, see figure 4, column 4, line 1-5) for defining electrical contact zones (contact zone of conduit 22 and pads 18, 20) providing double-sided electrical contacts for the space transformer; the contacts comprising: land grid array side contacts (20) disposed on the land grid array side of the silicon medium and semiconductor side contacts (18) disposed on the semiconductor side of the silicon medium.

Van fails to explicitly disclose land grid array side contacts have their largest dimension and their pitch in the order of mils to define a macro-pitch scale and semiconductor side contacts having their largest dimension and their pitch in the order of microns to define a micro-pitch scale. However, Van discloses a space transformer made of ceramic material, such as silicon, with land grid array side contacts (20) directly connected to the pads 72 of the substrate, (see description on column 3, line 56-64) and

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semiconductor side contacts (18) are directly connected to the pads 54 of the die 50, (column 3, line 41-49). This implies that space transformer of Van is converting the dimension of land grid array side contacts (20), which match to that of the substrate to the dimension of semiconductor side contacts (18), which match to that of semiconductor.

Further, Eldridge, in figure 4, discloses a space transformer 400, made of ceramic, bottom surface 402b with terminals at a 50-100 mil pitch, comparable to printed circuit board pitch, (land grid array side), defining macro-pitch scale, and top surface 402a with a relatively fine pitch, about 127 micron to 254 micron (5-10 mil pitch), center to center spacing comparable to semiconductor die bond pad, defining a micro-pitch scale, see column 23, line 5-25.

A person of ordinary skill in the art at the time the invention was made would readily construe that the dimension, size and spacing, on printed wiring board side, (land grid array side) would be larger, with wider pitch, defining macro-pitch scale, than that on the semiconductor side contacts of a space transformer, with narrower pitch, defining a micro-pitch scale, for connecting a semiconductor device on one side of the space transformer and a printed circuit board on the other side of the space transformer.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to construe the space transformer of Van, with land

grid array side contacts having dimensions and spacing larger, (defining macro-pitch scale), than that on the semiconductor side contacts, (defining a micro-pitch scale), from the teachings of Eldridge, in order to facilitate connection of the semiconductor device on one side and the printed circuit board on the other side of the space transformer.

Regarding the recitation, "the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly" and "the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly", the language "being configured to be connected to corresponding ones of contacts" only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, the modified structure of Van anticipates the claims.

8. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the modified structure of Van as applied to claims 10 and 14 above, and further in view of Petrarca et al., US Patent No. 6,429,522, hereafter, Petrarca and Matsuo et al., US Patent No. 6,614,106, hereafter, Matsuo.

Regarding claims 13 and 15, the combination of Van and Eldridge discloses all the features of the claimed invention as applied to claims 10 and 14 respectively, but fails to disclose an adhesion promoter disposed between the electrically conductive material and the first silicon layer.

Petrarca, in the background discussion, discloses that it is known in the semiconductor industry to apply an adhesion promotion layer such as silicon oxide, silicon nitride, titanium, tungsten or related compounds, before a metal deposition. The adhesion promotion layer is often used as a barrier for metal migration.

Matsuo discloses an interposer 30 made out of silicon substrate, column 2, line 35-50, and adhesion promotion layer for copper plating, column 3, line 23-30.

A person of ordinary skill in the art would readily recognize the advantage of providing adhesion promotion layer, before metal deposition, for better adhesion of the metal.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified structure of Van with adhesion promotion layer, from the teachings of Petrarca and Matsuo, in order to have better adhesion of the metal deposition.

Response to Arguments

9. Applicant's arguments filed on August 8, 2005 have been fully considered but they are not persuasive.

Regarding the rejection against the prior art of Yoda:

The applicant argues that Yoda fails to disclose "the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test

card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”

These are not found to be persuasive. As applied to claims 10-15, Yoda discloses the structure as claimed. Regarding the recitation, “the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”, the language “being configured to be connected to corresponding ones of contacts” only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, Yoda anticipates the claims.

Regarding the rejection against the prior art of Van and Eldridge:

The applicant argues that the modified structure of Van fails to disclose “the land grid array side contacts further being configured to be connected to corresponding ones of contacts of a test card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”

These are not found to be persuasive. As applied to claims 10-15, the modified structure of Van discloses the structure as claimed. Regarding the recitation, “the land grid array side contacts further being configured to be connected to corresponding ones

of contacts of a test card printed circuit board of a test card assembly” and “the semiconductor side contacts further being configured to be connected to corresponding ones of a probe head of the test card assembly”, the language “being configured to be connected to corresponding ones of contacts” only needs the contacts being able to be connected to the corresponding contacts, and does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138. Therefore, the modified structure of Van anticipates the claims.

Applicant further argues that Van discloses the spacing exactly opposite to that of the present invention. This is not found persuasive. A circuit board (70) is connected to one side and a semiconductor die (50) is connected to the other side of Van's structure (10). This arrangement, as shown in figure 4 of Van, shows that the spacing (20) of the contact on side connected to the circuit board is converted to that (18) suitable to be connected to a semiconductor die. As seen in figure 3b, the spacing (20) is greater than that (18) shown in figure 3A. Figure 4A is cross sectional view and does not disclose the actual spacing. The actual spacing is shown in Figure 3A and 3B, which are plan views. Therefore, the modified structure of Van anticipates the claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sporck et al., US Patent No. 6,856,150, in figure 6A, discloses a structure of a probe contact system.

Aldaz et al., US Patent No. 6,586,956, in figure 5, discloses a probe contact system.

Eldridge et al., US Patent No. 6,483,328, in figure 2, discloses a probe card for semiconductor devices.

11. Applicant's amendment necessitated the new explanations / ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
October 10, 2005